REMARKS

Applicant respectfully requests reconsideration. Claims 1-7 were previously pending in this application. By this amendment, claim 1 has been amended. As a result, claims 1-7 are pending for examination with claim 1 being an independent claim. No new matter has been added.

Applicant acknowledges the courtesies extended by Examiner Rao during a telephone interview with the undersigned on July 3, 2007. The substance of the interview is summarized in the remarks set forth herein below.

Rejections Under 35 U.S.C. §102

Claims 1-6 stand rejected under 35 U.S.C. §102 as being anticipated by Tuppen (U.S. Patent No. 5,279,687). Applicant respectfully traverses this rejection for at least the same reasons set forth in the prior response. Nevertheless, Applicant has amended claim 1 to further clarify the invention in an effort to advance prosecution of this application.

Independent claim 1 is directed to a method for forming, by epitaxy, a heteroatomic single-crystal semiconductor layer on a single-crystal semiconductor wafer, the crystal lattices of the layer and of the wafer being different. As amended, the method comprises first forming in the wafer surface, before epitaxy, at least one ring of discontinuities around a useful region of the wafer by forming at least one rough area in the wafer surface around the useful region. The method further comprises subsequently forming, by epitaxy, the heteroatomic single-crystal semiconductor layer directly on the wafer surface.

During the interview, the Examiner stated that he believed the term "ring of discontinuities" was unclear and overly broad. Applicant respectfully disagrees and maintains that the term "ring of discontinuities" is clear, particularly in view of the specification which sets forth that a discontinuity corresponds to a surface or groove irregularity. (See specification, p. 4, lines 25-27). During the interview, the Examiner asserted that the specification cannot be used to interpret the meaning of claim language. However, as explained during the interview, the definiteness of claim language must be analyzed, not in a vacuum, but in view of, *inter alia*, the specification. See MPEP 2173.02. Applicant respectfully submits that the term "ring of discontinuities" is clear and definite.

Following the interview, the Examiner further contended that claim 1 is unclear regarding the particular order of the formation of the discontinuities on the wafer surface and the formation of the epitaxial layer on the wafer surface. As indicated above, claim 1 has been amended in a manner believed to address the Examiner's concerns.

Tuppen is directed to preparing semiconductor substrates by annealing epitaxial layers in the form of mesas. As explained by Tuppen, annealing a secondary substrate formed by a primary wafer, such as a silicone wafer, and a mismatched epilayer, such as a Si/Ge alloy layer, relieves the strain created by the mismatch of cell sizes between the wafer and the epilayer.

In the Office Action and during the interview, the Examiner maintained that Tuppen purportedly discloses that the silicone wafer is prepared having an array of dislocations construing a roughened like surface area on the surface of the wafer prior to the epitaxial layering on top of the wafer substrate, and that this teaching would anticipate a ring of discontinuities. (Office Action, page 3, *citing* Tuppen, col. 2, lines 8-34). Applicant respectfully disagrees and respectfully submits that this portion of Tuppen is being misread.

As background information concerning the formation of semiconductor devices, Tuppen explains that the range of primary substrates for fabricating semiconductor devices is very limited because the crystallisation techniques used to prepare them are suitable only for a limited range of pure compounds and elements due to the cell sizes. (Col. 1, lines 8-23). As an example, Tuppen indicates that the use of alloys of Si/Ge as semiconductors would increase the range of operational properties for high speed circuits, but that it is not feasible to make Czochralski wafers out of Si/Ge alloys, making it necessary to grow Si/Ge alloy onto pure Si. (Col. 1, lines 24-29).

Tuppen explains that a mismatched wafer and epilayer substrate, such as a silicone wafer and a Si/Ge alloy epilayer, have different cell sizes that may lead to problems associated with growing an epilayer on a wafer. (Col. 1, lines 24-49). As the epilayer is much thinner than the wafer, the wafer will retain its normal structure and all the strain, which causes instability, will be imposed on the epilayer. (Col. 1, lines 50-62). When the epilayer thickness is below an equilibrium critical thickness, the strain energy is insufficient to cause dislocations in the epilayer. (Col. 1, lines 62-67). However, as the thickness of the epilayer increases above a metastable critical thickness, there is enough strain energy to cause the epilayer structure to dislocate. (col. 1, line 67 to col. 2, line 7). Such dislocations are generally in the form of

dislocation half loops comprising an interfacial component and two arms that thread up through the whole volume of the epitaxial layer, where the density of the dislocations in the epilayer depends on the degree of mismatch. (Col. 2, lines 8-14).

Applicant respectfully maintains that the dislocations described by Tuppen are not discontinuities formed by a rough area as recited in claim 1. Even were one of ordinary skill in the art to consider the dislocations described by Tuppen to be discontinuities in general, such dislocations occur within the epitaxial layer due to the strain energy created between the mismatched wafer and epilayer substrate. There is no teaching or suggestion that these dislocations are formed in the surface of the wafer. Moreover, Tuppen does not teach or suggest that these dislocations exist before the formation of any epitaxial layer on the wafer surface. Thus, Applicant respectfully submits that one of ordinary skill in the art would appreciate that the background section of Tuppen does not disclose first forming discontinuities by forming a rough area in the wafer surface prior to any epitaxial layer being formed on the wafer surface.

Recognizing the problems with dislocations associated with forming semiconductor devices with mismatched wafers and epilayers, Tuppen discloses two methods of forming a mismatched epilayer on a wafer.

In a first method, an unmasked substrate, e.g., a Czochralski wafer, is placed in an MBE or MOVPE growth chamber and a uniform epilayer which is different from the primary substrate is grown on the substrate. (Col. 6, lines 41-44). The substrate and the epilayer are removed from the growth chamber and a desired pattern of growth channels is produced, such as by using a saw or a scribe or by etching. (Col. 6, lines 44-47). After cutting, the wafer is returned to the growth chamber and annealed. (Col. 6, lines 47-49). As shown in FIG. 3B, in which the channels 22 are produced by cutting through a continuous layer of growth, the cuts may extend slightly below the surface of the wafer 20 so that the base of each channel 22 is formed by a groove 23 in the surface of the wafer 20. (Col. 5, lines 56-61). Thus, in the first method of Tuppen, the epilayer is first formed on the wafer surface, and then the grooves are subsequently formed through the epilayer and into the wafer surface. The grooves are ***not*** first formed in the wafer surface ***before*** the formation of the semiconductor layer directly on the wafer surface by epitaxy, as recited in claim 1.

In a second method, the primary wafer is masked, such as shown in FIG. 4, before introduction to the growth chamber. (Col. 6, lines 50-51). The masked substrate has areas 22

coated and windows 21 exposed for growth when the substrate is placed in the chamber. (Col. 6, lines 51-57). When the secondary substrate is complete, the substrate is annealed to relieve strain. (Col. 6, line 66 to col. 7, line 1). As shown in FIG. 3A, epitaxial mesas 22 are grown onto the wafer and are separated by channels 22, formed by the mask, which extend to the surface of the wafer. (Col. 5, lines 49-55). Thus, in the second method, there are no discontinuities at all formed in the wafer surface, let alone first forming discontinuities in the wafer surface before forming a semiconductor layer directly on the wafer surface by epitaxy, as recited in claim 1.

In view of the foregoing, claim 1 patentably distinguishes over Tuppen which does not disclose a method of forming, by epitaxy, a heteroatomic single-crystal semiconductor layer on a single-crystal semiconductor wafer by first forming in the wafer surface, before epitaxy, at least one ring of discontinuities around a useful region of the wafer by forming at least one rough area in the wafer surface around the useful region, and subsequently forming, by epitaxy, the heteroatomic single-crystal semiconductor layer directly on the wafer surface as recited in claim 1. Accordingly, the rejection of claim 1 as being anticipated by Tuppen is improper and should be withdrawn.

Claims 2-6 depend from claim 1 and are patentable for at least the same reasons and novel features recited therein. Accordingly, withdrawal of this rejection is respectfully requested.

Claim 5 further recites that the roughness of the rough area on the wafer surface exhibits a mean square deviation ranging between 10 and 30 nm. In the Office Action, the Examiner contends that this roughness is met by Tuppen which discloses that the density of the threading dislocations in the epilayer generally lies in the range of $10^6 - 10^{10}$ cm^{-2}. (Office Action, pages 3-4). Applicant respectfully submits that the density of dislocations (i.e., the number of dislocations per unit area) is completely unrelated to the roughness of a surface. Tuppen does not teach or suggest any area on the wafer surface having a roughness as recited in claim 5. Accordingly, withdrawal of the rejection of claim 5 is respectfully requested for at least this additional reason.

Rejections Under 35 U.S.C. §103

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Tuppen in view of Masato (JP 2002-359189).

Without acceding to the propriety of the combination suggested in the Office Action, claim 7 depends indirectly from claim 1 and is patentable for at least the same reasons set forth above. Accordingly, withdrawal of this rejection is respectfully requested.

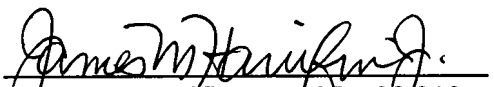
CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes that the application is not in condition for allowance, the Examiner is requested to call the undersigned at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: July 6, 2007

Respectfully submitted,

By: 

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